REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

As a preliminary matter, the Applicant acknowledges with appreciation the allowance of claims 9-14 of the present application.

By the foregoing amendments, claim 1 has been amended, and new claims 15 and 16 have been added. No new matter has been added. Thus, claims 1-8 and 15-16 are currently pending in the application and subject to examination, claims 9-14 having been allowed.

In the Office Action mailed June 29, 2004, the Examiner objected to claim 1 due to informalities. Claim 1 has been amended responsive to this rejection. No further amendment is necessary at this time.

The Examiner rejected claims 3-8 under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is respectfully traversed, as follows. In Fig. 2 of the present application, dashed line L1 supplies the phase synchronized clock generating circuit 6 with external input data DATA (external clock CLK 1), which in turn supplies phase comparator 7 with a comparison clock CLK 3, phase synchronized to the external input data DATA. Dashed line L2 supplies the phase synchronized clock generating circuit 6 to the internal clock CLK 2, which in turn supplies phase comparator 7 with a comparison clock CLK 3, phase synchronized with the internal clock CLK 2. This is described in further detail on page 10, line 24 through page 11, line 16 of the specification. If any additional clarification or amendment is necessary to overcome this

rejection, the Examiner is requested to contact the Applicant's undersigned representative.

The Examiner rejected claims 1 and 2 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,249,160 to Tagami et al. It is noted that claim 1 has been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicant hereby traverses the rejection, as follows.

Tagami et al. discloses a control signal supplied to a VCO, the control signal generated on the basis of an output signal of one phase detector (phase comparator) 2. It is noted that in Tagami et al. (*see, e.g.*, Fig. 5), phase detector 13 receives a clock phase output (CLOCK OUT) and outputs a control signal only to control the delay value of a variable delay circuit 12.

Nothing in Tagami et al., however, teaches or suggests at least the feature of a control signal being generated based on phase difference detection information from at least one of a plurality of phase detection units and at least one of the other of the plurality of phase detection units, as recited in claim 1, as amended.

For at least this reason, the Applicant submits that claim 1, as amended, is allowable over the cited prior art. As claim 1, is allowable, the Applicant submits that claims 2-8 and 15, which depend from allowable claim 1, are likewise allowable over the cited prior art.

Furthermore, nothing in Tagami et al., teaches or suggests at least the features of a phase difference detection circuit comprising a plurality of phase detection units, at least one of the plurality of phase detection units carrying out a direct phase detection in which a phase of the clock is directly compared with the phase of the reference

waveform, and at least one of the other of the plurality of phase detection units carrying out an indirect phase detection by detecting a phase difference between the clock and a data clock synchronized to the externally supplied data using a phase-synchronized waveform generating circuit generating a waveform synchronized in phase with the reference waveform or an output of the clock generating circuit and a phase information extracting circuit extracting phase information from the phase-synchronized waveform, as recited in new claim 16.

For at least this reason, the Applicant submits that new claim 16 is allowable over the cited prior art.

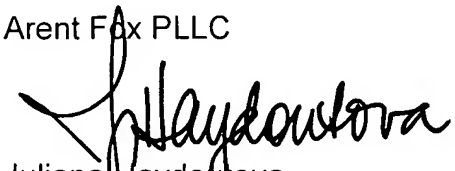
For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referring to client-matter number 100021-00131.

Respectfully submitted,

Arent Fox PLLC



Juliana Haydoutova
Attorney for Applicants
Registration No. 43,313

Customer No. 004372
1050 Connecticut Ave., N.W.
Suite 400
Washington, D.C. 20036-5339
Telephone No. (202) 715-8469
Facsimile No. (202) 638-4810

JH:ksm

Enclosures: Petition for Extension of Time (two months)